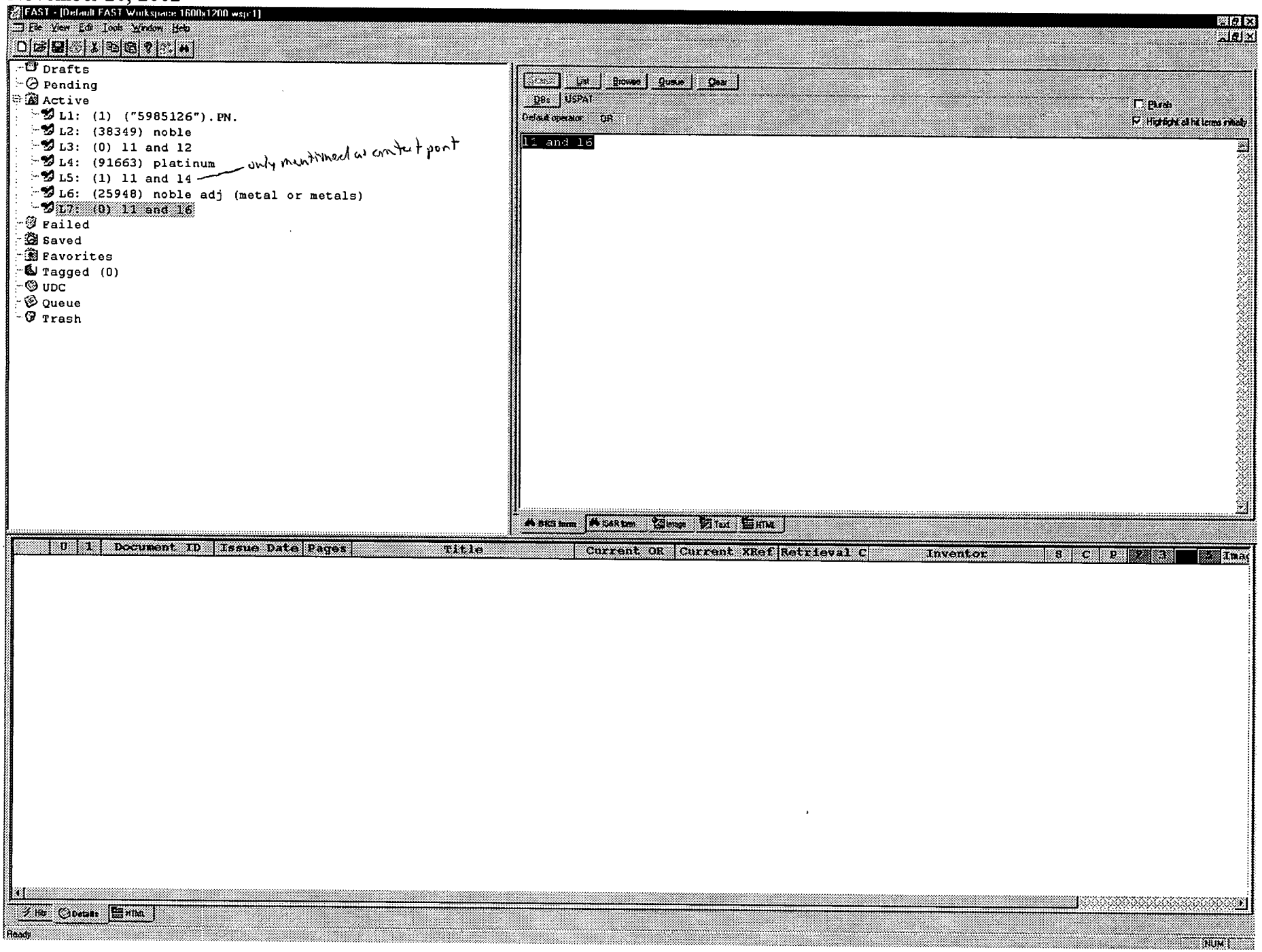
November 20, 2002



11/2002

201.09 Substitute Application

The use of the term "Substitute" to designate any application which is in essence the duplicate of an application by the same applicant abandoned before the filing of the later application, finds official recognition in the decision *Ex parte Komenak*, 1940 C.D. 1, 512 O.G. 739 (Comm'r Pat. 1940). Current practice does not require applicant to insert in the specification reference to the earlier application; however, attention should be called to the earlier application. The notation on the file wrapper (see MPEP § 202.02) that one application is a "Substitute" for another is printed in the heading of the patent copies. See MPEP § 202.02.

As is explained in MPEP § 201.11, a "Substitute" does not obtain the benefit of the filing date of the prior application.

Use form paragraph 2.07 to remind applicant of possible substitute status.

¶ *2.07 Definition of a Substitute*
Applicant refers to this application as a "substitute" of Application No. **[1]**, filed **[2]**. The use of the term "substitute" to designate an application which is in essence the duplicate of an application by the same applicant abandoned before the filing of the later case finds official recognition in the decision, *Ex parte Komenak*, 1940 C.D. 1, 512 O.G. 739 (Comm'r Pat. 1940). The notation on the file wrapper (See MPEP § 202.02) that one case is a "substitute" for another is printed in the heading of the patent copies. A "substitute" does not obtain the benefit of the filing date of the prior application.

201.10 Refile

No official definition has been given the term "Refile," though it is sometimes used as an alternative for the term "Substitute."

If the applicant designates his or her application as "Refile" and the examiner finds that the application is in fact a duplicate of a former application by the same party which was abandoned prior to the filing of the second application, the examiner should require the substitution of the word "substitute" for "refile", since the former term has official recognition.

Use form paragraph 2.08 to remind applicant of possible refile status.

¶ *2.08 Definition of a Refile*
It is noted that applicant refers to this application as a "refile." No official definition has been given the term "refile," though it is sometimes used as an alternative for the term "substitute." Since this application appears to be in fact a duplicate of a former application which was abandoned prior to the filing of the second case, the substitution of the word "substitute" for "refile" is required since the term "substitute" has official recognition. Applicant is required to make appropriate corrections.

MPEP
201.11 Continuity Between Applications: When Entitled to Filing Date

Under certain circumstances an application for patent is entitled to the benefit of the filing date of a prior nonprovisional application or provisional application which has at least one common inventor. The conditions are specified in 35 U.S.C. 120 and 35 U.S.C. 119(e).

35 U.S.C. 120. Benefit of earlier filing date in the United States.
An application for patent for an invention disclosed in the manner provided by the first paragraph of section 112 of this title in an application previously filed in the United States, or as provided by section 363 of this title, which is filed by an inventor or inventors named in the previously filed application shall have the same effect, as to such invention, as though filed on the date of the prior application, if filed before the patenting or abandonment of or termination of proceedings on the first application or on an application similarly entitled to the benefit of the filing date of the first application and if it contains or is amended to contain a specific reference to the earlier filed application. No

application shall be entitled to the benefit of an earlier filed application under this section unless an amendment containing the specific reference to the earlier filed application is submitted at such time during the pendency of the application as required by the Director. The Director may consider the failure to submit such an amendment within that time period as a waiver of any benefit under this section. The Director may establish procedures, including the payment of a surcharge, to accept an unintentionally delayed submission of an amendment under this section.

35 U.S.C. 119. Benefit of earlier filing date; right of priority.

*****

(e)

(1) An application for patent filed under section 111(a) or section 363 of this title for an invention disclosed in the manner provided by the first paragraph of section 112 of this title in a provisional application filed under section 111(b) of this title, by an inventor or inventors named in the provisional application, shall have the same effect, as to such invention, as though filed on the date of the provisional application filed under section 111(b) of this title, if the application for patent filed under section 111(a) or section 363 of this title is filed not later than 12 months after the date on which the provisional application was filed and if it contains or is amended to contain a specific reference to the provisional application. No application shall be entitled to the benefit of an earlier filed provisional application under this subsection unless an amendment containing the specific reference to the earlier filed provisional application is submitted at such time during the pendency of the application as required by the Director. The Director may consider the failure to submit such an amendment within that time period as a waiver of any benefit under this subsection. The Director may establish procedures, including the payment of a surcharge, to accept an unintentionally delayed submission of an amendment under this subsection during the pendency of the application

(2) A provisional application filed under section 111(b) of this title may not be relied upon in any proceeding in the Patent and Trademark Office unless the fee set forth in subparagraph (A) or (C) of section 41(a)(1) of this title has been paid.

(3) If the day that is 12 months after the filing date of a provisional application falls on a Saturday, Sunday, or Federal holiday within the District of Columbia, the period of pendency of the provisional application shall be extended to the next succeeding secular or business day.

There are six conditions for receiving the benefit of an earlier filing date under 35 U.S.C. 120 or under 35 U.S.C. 119(e).

(A) The second application must be an application for a patent for an invention which is also disclosed in the first application (the parent or original nonprovisional application or provisional application); the disclosure of the invention in the first application and in the second application must be sufficient to comply with the requirements of the first paragraph of 35 U.S.C. 112. See *Transco Prods., Inc. v. Performance Contracting, Inc.*, 38 F.3d 551, 32 USPQ2d 1077 (Fed. Cir. 1994). Form paragraphs 2.09 and 2.10 should be used where the disclosure of the second application is not for an invention disclosed in the first application.

¶ 2.09 Heading for Conditions for Domestic Priority Under 35 U.S.C. 119(e) or 120

Applicant has not complied with one or more conditions for receiving the benefit of an earlier filing date under 35 U.S.C. **[1]** as follows:

Examiner Note

1.

In bracket 1, insert either or both --119(e)-- or --120--.

2.

One or more of the following form paragraphs 2.10 to 2.12 must follow depending upon the circumstances.

¶ 2.10 Disclosure Must Be the Same

The second application must be an application for a patent for an invention which is also disclosed in the first application (the parent or provisional application); the disclosure of the invention in the parent application and in the second application must be sufficient to

WRITTEN OPINION

Form PCT/IPEA/408 (Box V) (July 1998)
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International application No.
PCT/US00/29440

V. Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. statement

Novelty (N)	Claims	1-43	YES
	Claims	NONE	NO
Inventive Step (IS)	Claims	5-7, 14, 38-42	YES
	Claims	1-4, 8-13, 15-37, 43	NO
Industrial Applicability (IA)	Claims	1-43	YES
	Claims	NONE	NO

2. citations and explanations

Claims 1, 3, 35, 37 and 43 lack an inventive step under PCT Article 33(3) as being obvious over Zila et al (US 5,731,678 A) in view of Katou (US 5,344,491 A).

The Zila et al patent is directed to apparatus, shown in figure 2, for electroplating onto a semiconductor wafer. The apparatus is capable of electroplating material onto one surface of the wafer which is immersed in the electroplating solution while not exposing the opposite surface (column 1, lines 35-42). The apparatus includes a workpiece support with fingers 848 which provide electroplating power to the wafer at a plurality of discrete contact points about the periphery of the wafer as recited in instant claim 1. See figures 16-19, and column 15, line 30 to column 17, line 25. Seal 868 seals the electrode contact (column 19, lines 21-38).

The workpiece support is part of movable processing head 406 which spins about axis 410 (column 5, lines 50-57). The processing head includes an actuator which moves the head between a loading position, shown in figure 3, and a processing position, shown in figure 5, as recited in instant claim 3 (column 6, lines 3-46).

Applicant's claimed invention as recited in independent claims 1, 3 and 35 differs from the apparatus of Zila et al by reciting that the electroplating solution contains a noble metal and that an anode spaced from the workpiece support is provided. The Katou patent discloses a method and apparatus for electroplating a thin metal layer onto a semiconductor wafer 1 in which the wafer is positioned with the surface to be plated face down and exposed to the electroplating solution 4. Anode 7 is spaced from the workpiece within the electroplating solution (figure 2). One of the metals that may be plated is gold, a noble metal (column 5, line 10).

Applicant's claimed invention lacks an inventive step since it would have been obvious to have provided noble metal-containing electroplating solution in the apparatus of Zila et al because a noble metal such as gold is useful as a deposited layer on a semiconductor wafer as taught by Katou. It would additionally have been obvious to have provided an anode in the apparatus of Zila et al as shown by Katou to complete the circuit (Continued on Supplemental Sheet.)

Note newly cited references (page 12)

Supplemental Box
(To be used when the space in any of the preceding boxes is not sufficient)

Continuation of: Boxes I - VIII

TIME LIMIT:

The time limit set for response to a Written Opinion may not be extended. 37 CFR 1.484(d). Any response received after the expiration of the time limit set in the Written Opinion will not be considered in preparing the International Preliminary Examination Report.

CLASSIFICATION:

The International Patent Classification (IPC) and/or the National classification are as listed below:
IPC(7): C25D 3/50, 5/02, 5/18, 7/12, 17/00, 21/06; H01L 21/288 and US Cl.: 204/199, 224R, 238; 205/123, 210, 264; 438/618

V. 2. REASONED STATEMENTS - CITATIONS AND EXPLANATIONS (Continued):
supplying electroplating power to the semiconductor wafer.

With respect to claim 37, figure 2 of Katou shows taht the anode is in the form of a mesh through which the electroplating solution flows. The openings in the mesh serve as individual nozzles which provide fluid flow components to distribute the electroplating solution over the wafer as recited in instant claim 37. With respect to claim 43, there appears to be no separation of the electroplating solution of Katou as it flows toward the upper portion of the plating cup.

Claims 2, 4 and 36 lack an inventive step under PCT Article 33(3) as being obvious over the prior art as applied in the immediately preceding paragraph and further in view of Inoue et al (US 5,556,814 A).

Claims 2, 4 and 36 recite that the electroplating solution includes platinum for deposition on the workpiece. As noted above, Katou discloses that one of the metals that may be plated is gold. The Inoue et al patent is directed to the deposition of a metal layer on integrated circuits by electroplating. Inoue et al disclose that the electroplated metal may be copper, gold, platinum or palladium (column 6, lines 34-38). The claimed invention lacks an inventive step since it would have been obvious to have provided platinum in the electroplating solution of Zila et al because platinum is recognized as an equivalent to gold as shown by Inoue et al.

Claims 8 and 10-13 lack an inventive step under PCT Article 33(3) as being obvious over Zila et al (US 5,731,678 A) in view of Katou (US 5,344,491 A) as applied to claims 1, 3, 35, 37 and 43 above, and further in view of Tsuda et al (US 4,243,532 A) and Owczarz et al (US 5,232,328 A).

Zila et al and Katou are interpreted as above. Claim 8 additionally recites a chemical delivery system for supplying and recirculating electroplating solution and a multi-stage filtration system. Katou discloses a system for supplying electroplating solution to the plating chambers and recirculating the electroplating solution through filters 11. Katou does not specify multi-stage filtration. The Tsuda et al patent discloses apparatus in which a fluid is filtered. Tsuda et al teach that a plurality of filters having different pore sizes are placed within the flow path where the first filter has a large pore size to prevent large particles from flowing out and a successive filter has a smaller pore size to prevent finer powders from flowing out. By using this arrangement, clogging of the filter mesh becomes less frequent (column 5, line 57 to column 6, line 3). Choice of filter mesh sizes would have depended on size of particles determined to be detrimental to the process being carried out and the clogging frequency of the filters. This is illustrated by the Owczarz et al patent which is directed to apparatus for semiconductor processing. Owczarz et al suggest providing a first filter with an approximate pore size of 1 micron and a second filter with an approximate pore size of 0.1-0.2 microns to reduce introduction of contaminant particles into the processing chamber (column 18, lines 10-16). The claimed invention lacks an inventive step since it would have been obvious to have utilized multi-stage filtration in the apparatus of Owczara et al as taught by Tsuda et al and Owczarz et al because clogging of the filter would have been less frequent and contamination of the process by fine particles would have been reduced.

Claim 9 lacks an inventive step under PCT Article 33(3) as being obvious over the prior art as applied in the immediately preceding paragraph and further in view of Inoue et al (US 5,556,814 A).

Inoue et al is interpreted as above. Claim 9 recites that the electroplating solution includes platinum for deposition on the workpiece. The claimed invention lacks an inventive step since it would have been obvious to have provided platinum in the electroplating solution of Zila et al because platinum is recognized as an equivalent to gold as shown by Inoue et al.

Supplemental Box
(To be used when the space in any of the preceding boxes is not sufficient)

Continuation of: Boxes I - VIII

Claim 15 lacks an inventive step under PCT Article 33(3) as being obvious over Katou (US 5,344,491 A) in view of Dubin (US 5,972,192 A) and either of the Lowenheim text *Elecroplating* or Goldberg (US 5,484,518 A).

As noted aobve, the Katou patent discloses a method for electroplating a thin metal layer onto a semiconductor wafer 1 in which the wafer is positioned with the surface to be plated face down and exposed to the electroplating solution 4. Anode 7 is spaced from the workpiece within the electroplating solution. Electroplating power is supplied between cathode 3, connected to wafer 1, and anode 7. See figure 2 and column 3, lines 15-27. One of the metals that may be plated is gold, a noble metal (column 5, line 10).

Applicant's claimed process differs from the method of Katou by reciting application of electroplating power using a low current density for a first period of time and the subsequent application of higher current for a second period of time. The Dubin patent is directed to a process for electroplating a layer of metal onto a semiconductor wafer. Dubin teaches that a thin seed layer is required on the surface of the wafer to carry current for electroplating (column 4, lines 19-21). The Lowenheim text discusses for electroplating workpieces on which a thin conductive layer has been deposited to carry electroplating current. Lowenheim teaches that the surface does not have the electrical conductivity of massive metals, so that electroplating must be started at low current densities until a fair thickness of electrodeposit is built up (page 418). The Goldberg is patent is directed to a process of electroplating in which a thin conductive coating to carry electroplating current is first formed. Goldberg teaches that theoretically, a low initial current density should be prefered with current density increased as an initial deposit is formed, to prevent burn off of the thin coating (column 8, lines 15-19).

The prior art is indicative of the level of skill of one of ordinary skill in the art. The claimed invention lacks an inventive step since it would have been obvious to have performed the electroplating process of Katou by providing a seed layer as taught by Dubin because this layer would have provided electrical conductivity sufficient for electroplating to the surface of the workpiece, and to have used a low current density for a first period of time and then to have increased the current density as taught by Lowenheim and Goldberg because the low current density would have electrodeposited metal onto the surface slowly without burning the seed layer, and the subsequent current density would have allowed faster plating to reduce process time.

Claims 16-19 and 32-34 lack an inventive step under PCT Article 33(3) as being obvious over the prior art as applied in the immediately preceding paragraph and further in view of Young et al (US 4,705,606 A).

Claims 16-19 and 32-34 additionally differ by reciting pre-treatment before electroplating and spinning to remove electroplating solution. The Young et al patent is directed to electroplating electrical connections on integrated circuits. Young et al teach that the substrate should be prepared before electroplating (column 3, lines 25-45). Preparation may include rinsing in deionized water. Following treatment the wafer is spun dry. The substrate may also be treated in an acidic solution. The claimed invention lacks an inventive step since it would have been obvious to have pretreated the wafer in the electroplating process of Katou by rinsing in deionized water or an acidic solution and removing process liquids by spinning as taught by Young et al because contaminants on the wafer surface would have been removed and the wafer would have been dried.

Claim 20 lacks an inventive step under PCT Article 33(3) as being obvious over Katou (US 5,344,491 A) in view of Dubin (US 5,972,192 A) and either of the Lowenheim text *Elecroplating* or Goldberg (US 5,484,518 A), as applied to claim 15 above, and further in view of Inoue et al (US 5,556,814 A).

Katou, Dubin, Lowenheim and Goldberg are interpreted as above. Claim 20 recites that the electroplating solution includes platinum for deposition on the workpiece. As noted above, Katou discloses that one of the metals that may be plated is gold, and the Inoue et al disclose that the electroplated metal may be copper, gold, platinum or palladium (column 6, lines 34-38). The claimed invention lacks an inventive step since it would have been obvious to have deposited platinum in the process of Katou because platinum is recognized as an equivalent to gold as shown by Inoue et al.

Claims 21-31 lack an inventive step under PCT Article 33(3) as being obvious over the prior art as applied in the immediately preceding paragraph and further in view of Abys (US 4,427,502 A). Claims 21-31 relate to process parameters used in the electrodeposition of platinum. The Abys patent is directed to a process for electroplating platinum and platinum alloys. The platinum concentraiton ranges from 0.005 molar to saturation (column 4, lines 40-41). This range includes the range recited in instant claim 21. The pH is preferably within the range of 10 to 12.5 (column 3, lines 53-57). This range includes the range of 11-12 recited in claim 24. Abys discloses that a preferred temperature range is 50° to 70° C. This range falls within the range of 40-80° C recited in claim 22 and includes 65°C as recited in claim 23. The Lowenheim text discloses a number of plating baths useful for platinum plating. In addition to alkaline bath U similar to that of Abys, Lowenheim discloses that acidic baths can be used. Bath T has a pH of 2 which falls within the range recited in instant claim 27. The amount of platinum in this bath is 5 g/l which falls within the range recited instant claim 28.

International application No.
PCT/US00/29440

Supplemental Box
(To be used when the space in any of the preceding boxes is not sufficient)

Continuation of: Boxes I - VIII

Abys discloses the use of a broad current density range including less than 50 ASF for low speed plating and 50-1000 ASF for high speed plating (column 4, lines 43-45). A current of 50 ASF approximately equals 50 mA/cm^2. Lowenheim discloses current densities ranging from 40-140 A/m^2 (4-14 mA/cm^2). Neither Abys nor Lowenheim discloses the use of pulse current. Dubin et al disclose that pulse current as recited in instant claims 25 and 30 may advantageously be used for electroplating into the surface features of a semiconductor wafer. See the abstract. In the examples, Dubin et al use a plating current density in the range of 5-50 mA/cm^2. This range includes values similar to those disclosed by Abys and Lowenheim, and overlaps the ranges recited in instant claims 26 and 29. In example 1, a pulse frequency of about 1 to about 1000 Hz (1 to 1000 milliseconds) and a duty cycle of about 10% to about 90% was used. These ranges include the pulse parameters recited in instant claim 31.

Applicant's claimed invention lacks an inventive step since it would have been obvious at the time the invention was made to have utilized process parameters for the electrodeposition of platinum which are shown to be conventional by Abys, Lowenheim and Dubin because the semiconductor wafer would have been effectively plated.

Claims 5-7, 14 and 38-42 meet the criteria set out in PCT Article 33(2)-(3), because the prior art does not teach or fairly suggest a contact member for conducting electroplating power to a microelectronic workpiece which includes a removable conductive surface material disposed about an exterior surface of a conductive member.

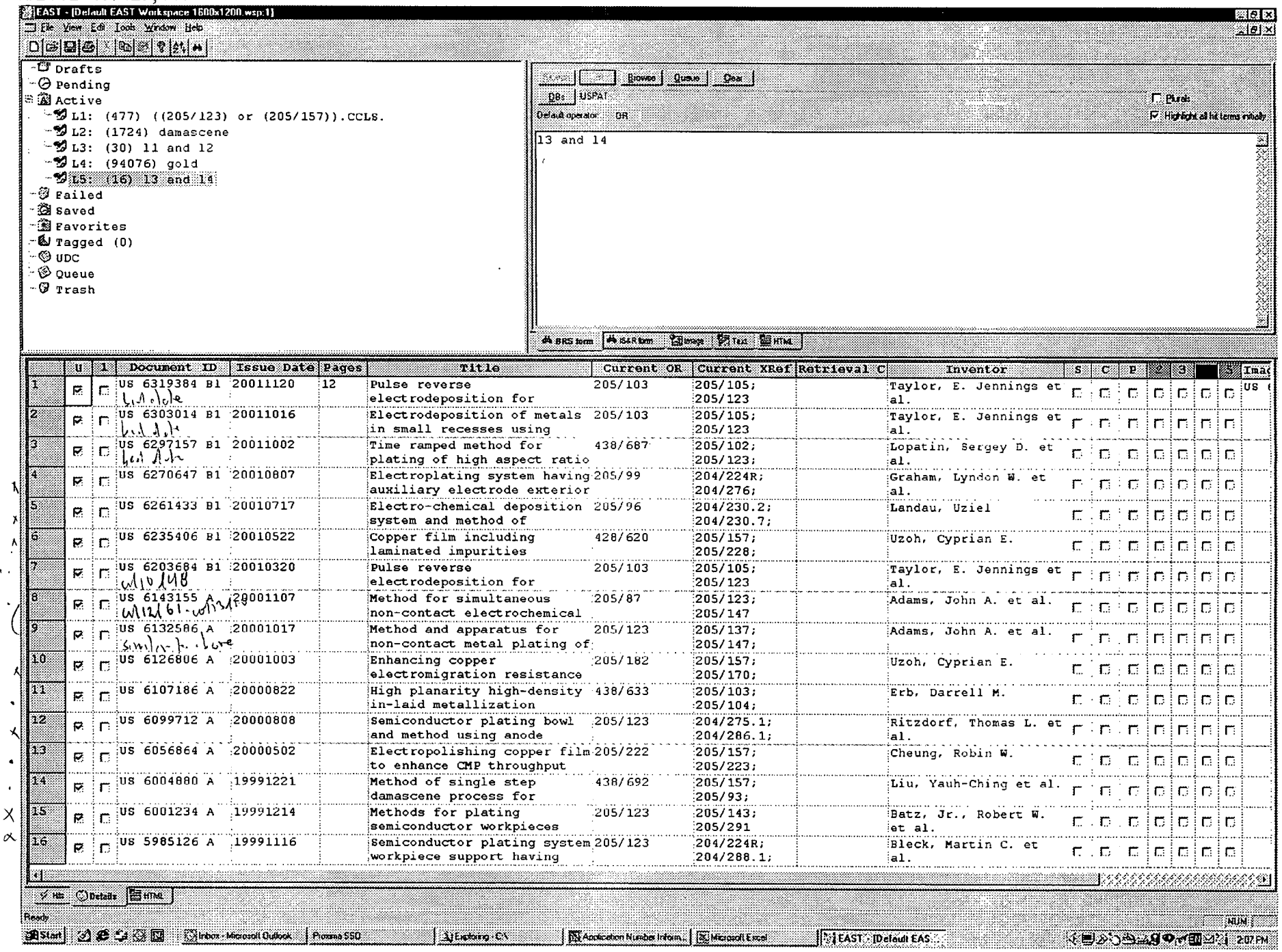
Claim 14 meets the criteria set out in PCT Article 33(2)-(3), because the prior art does not teach or fairly suggest the apparatus as recited for plating a noble metal or alloy on a microelectronic workpiece, the apparatus including a disposable current thief which comprises conductive portions of a printed circuit board.

Claim 38-42 meet the criteria set out in PCT Article 33(2)-(3), because the prior art does not teach or fairly suggest the apparatus as recited in claim 37 which additionally includes the specific features of these dependent claims.

Claims 5-7, 14 and 38-42 meet the criteria set out in PCT Article 33(4), because the claimed subject matter has industrial applicability in the field of semiconductor processing.

---------- NEW CITATIONS ----------

US 4,243,532 A (TSUDA et al) 06 January 1981, column 5, line 57-column 6, line 3.
US 5,232,328 A (OWCZARA et al) 03 August 1993, column 18, lines 10-16.
US 5,344,491 A (KATOU) 06 September 1994, figure 2.
US 5,484,518 A (GOLDBERG) 16 January 1996, column 8, lines 13-29.
US 5,731,678 A (ZILA et al) 24 March 1998, abstrract.



	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval C	Inventor	S	C	P	2	3		5	Imac
1	☑	☐	US 6319384 B1	20011120	12	Pulse reverse electrodeposition for	205/103	205/105; 205/123		Taylor, E. Jennings et al.	☐	☐	☐	☐	☐	☐	☐	US
2	☑	☐	US 6303014 B1	20011016		Electrodeposition of metals in small recesses using	205/103	205/105; 205/123		Taylor, E. Jennings et al.	☐	☐	☐	☐	☐	☐	☐	
3	☑	☐	US 6297157 B1	20011002		Time ramped method for plating of high aspect ratio	438/687	205/102; 205/123;		Lopatin, Sergey D. et al.	☐	☐	☐	☐	☐	☐	☐	
4	☑	☐	US 6270647 B1	20010807		Electroplating system having auxiliary electrode exterior	205/99	204/224R; 204/276;		Graham, Lyndon W. et al.	☐	☐	☐	☐	☐	☐	☐	
5	☑	☐	US 6261433 B1	20010717		Electro-chemical deposition system and method of	205/96	204/230.2; 204/230.7;		Landau, Uziel	☐	☐	☐	☐	☐	☐	☐	
6	☑	☐	US 6235406 B1	20010522		Copper film including laminated impurities	428/620	205/157; 205/228;		Uzoh, Cyprian E.	☐	☐	☐	☐	☐	☐	☐	
7	☑	☐	US 6203684 B1	20010320		Pulse reverse electrodeposition for	205/103	205/105; 205/123		Taylor, E. Jennings et al.	☐	☐	☐	☐	☐	☐	☐	
8	☑	☐	US 6143155 A	20001107		Method for simultaneous non-contact electrochemical	205/87	205/123; 205/147		Adams, John A. et al.	☐	☐	☐	☐	☐	☐	☐	
9	☑	☐	US 6132586 A	20001017		Method and apparatus for non-contact metal plating of	205/123	205/137; 205/147;		Adams, John A. et al.	☐	☐	☐	☐	☐	☐	☐	
10	☑	☐	US 6126806 A	20001003		Enhancing copper electromigration resistance	205/182	205/157; 205/170;		Uzoh, Cyprian E.	☐	☐	☐	☐	☐	☐	☐	
11	☑	☐	US 6107186 A	20000822		High planarity high-density in-laid metallization	438/633	205/103; 205/104;		Erb, Darrell M.	☐	☐	☐	☐	☐	☐	☐	
12	☑	☐	US 6099712 A	20000808		Semiconductor plating bowl and method using anode	205/123	204/275.1; 204/286.1;		Ritzdorf, Thomas L. et al.	☐	☐	☐	☐	☐	☐	☐	
13	☑	☐	US 6056864 A	20000502		Electropolishing copper film to enhance CMP throughput	205/222	205/157; 205/223;		Cheung, Robin W.	☐	☐	☐	☐	☐	☐	☐	
14	☑	☐	US 6004880 A	19991221		Method of single step damascene process for	438/692	205/157; 205/93;		Liu, Yauh-Ching et al.	☐	☐	☐	☐	☐	☐	☐	
15	☑	☐	US 6001234 A	19991214		Methods for plating semiconductor workpieces	205/123	205/143; 205/291		Batz, Jr., Robert W. et al.	☐	☐	☐	☐	☐	☐	☐	
16	☑	☐	US 5985126 A	19991116		Semiconductor plating system workpiece support having	205/123	204/224R; 204/288.1;		Bleck, Martin C. et al.	☐	☐	☐	☐	☐	☐	☐	

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	Document ID	Pages	1	2	3	4	5	U	S	C	P	Kind Codes	Sou
2	US 6303014 B1	24						☑					USPAT
3	US 6297157 B1	9						☑					USPAT
4	US 6270647 B1	20						☑					USPAT
5	US 6261433 B1	22						☑					USPAT
6	US 6235406 B1	15						☑					USPAT
7	US 6203684 B1	11							☑				USPAT
8	US 6143155 A	17						☑					USPAT

metal deposited in the trenches.

DEPR:
FIG. 4A illustrates schematically a cross-section of a semiconductor wafer that has been cut from a single crystal of a semiconductor, e.g., silicon. Such wafers are typically round and very thin. In order to metallize the surface of the wafer a barrier layer (not shown) and a very thin conducting layer (not shown) are deposited, e.g., by CVD, as for the case of the damascene -prepared surface discussed above.

DEPR:
FIG. 4B shows an enlarged cross section of the edge of the wafer 400 as indicated by the circle 4B in FIG. 4A. A metal layer 406 is shown schematically and with exaggerated thickness as deposited on the surface 402 of the wafer 400 near its edge 404 after the first, relatively short, cathodic current pulse. As discussed above for the damascene -prepared surface, because the cathodic pulse is of finite duration, there may be some non-uniformity in the deposition of the metal layer, as shown by the excess metal 408 deposited at the edge 404 of the wafer 400.

DEPR:
The method of the invention may be used with any metal that can be deposited by electroplating techniques. Thus copper, silver, gold, zinc, chromium, nickel, and alloys thereof such as bronze, brass, and the like, may be applied to microrough surfaces by the process of the invention. The invention is particularly useful in filling trenches and vias in damascene -prepared surfaces generated in the manufacture of VLSI semiconductor devices and the like and in preparing planar layers of metal on large-diameter semiconductor wafers.

DEPR:
The electroplating bath used in the process of the invention can be any conventional electroplating bath appropriate for the metal being plated. For electroplating copper onto a semiconductor surface, particularly when preparing microscopic conductors by the damascene process, it is preferred to avoid conventional additives such as leveling agents and the like to the extent possible, in order to avoid the difficulties of using such additives such as possible inclusion in the plated conductors. A preferred bath for electroplating copper onto a microrough surface is an aqueous acidic copper sulfate bath incorporating about 40 to about 80 g/L of copper sulfate, a molar ratio of sulfuric acid to copper sulfate of about 5:1 to about 8:1, about 5% of polyethylene glycol and about 30 ppm to about 60 ppm of chloride ion. A pulse train frequency of about 1000 Hz with a cathodic duty cycle of about 20%, an anodic duty cycle of about 75% and a cathodic/anodic charge transfer ratio of 5 or less appeared to give superior results.

CLPR:
15. The method of claim 1 wherein said metal is selected from the group consisting of copper, silver, gold, zinc, chromium, nickel, bronze, brass, and alloys thereof.

CCXR:
205/123

c/4 154 less than 1-2 mm trenches

(12) **United States Patent**
Taylor et al.

(10) **Patent No.: US 6,203,684 B1**
(45) **Date of Patent: Mar. 20, 2001**

(54) **PULSE REVERSE ELECTRODEPOSITION FOR METALLIZATION AND PLANARIZATION OF A SEMICONDUCTOR SUBSTRATES**

(75) Inventors: E. Jennings Taylor, Troy, OH (US); Chengdong Zhou, Salem, OR (US); Jenny J. Sun, Tipp City, OH (US)

(73) Assignee: Faraday Technology Marketing Group, LLC, Troy, OH (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/172,299

(22) Filed: Oct. 14, 1998

(51) Int. Cl.[7] C25D 5/18

(52) U.S. Cl. 205/103; 205/105; 205/123

(58) Field of Search 205/103, 105, 205/123

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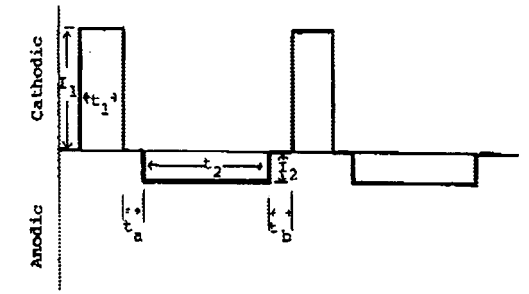
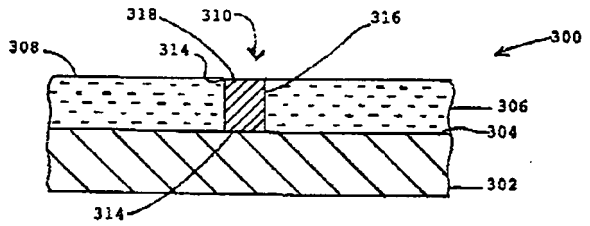
Primary Examiner—Kathryn Gorgos
Assistant Examiner—Wesley A. Nicolas
(74) *Attorney, Agent, or Firm*—Vorys, Sater, Seymour and Pease LLP

(57) **ABSTRACT**

A smooth layer of a metal is electroplated onto a microrough electrically conducting substrate by immersing the substrate and a counterelectrode in an electroplating bath of the metal to be electroplated and passing a modulated reversing electric current between the electrodes. The current contains pulses that are cathodic with respect to said substrate and pulses that are anodic with respect to said substrate. The cathodic pulses have a duty cycle less than about 50% and said anodic pulses have a duty cycle greater than about 50%, the charge transfer ratio of the cathodic pulses to the anodic pulses is greater than one, and the frequency of said pulses ranges from about 10 Hertz to about 5000 Hertz.

21 Claims, 4 Drawing Sheets





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3	US 6297157 B1	9							x				USPAT
4	US 6270647 B1	20							x				USPAT
5	US 6261433 B1	22							x				USPAT
6	US 6235406 B1	15							x				USPAT
7	US 6203684 B1	11							x				USPAT
	US 6143155 A	17							x				USPAT
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5,344,539, Shinogi et al., were reduced to a single potential, a simpler and more reliable system would result. The present invention accomplishes all of these goals.

DEPR:
As mentioned, the present implementation of the invention is a system to process 300 mm diameter or smaller semiconductor wafers. There is no practical limiting feature that would prevent the design of a system utilizing the present invention for use with 400 or 500 mm wafers or larger, or with rectangular objects such as flat panel displays. In addition, our current invention could easily utilize the same process on any material that had a conductive seed layer and feature trenches and vias, such as decorative damascene inlays, damascene structures used in printed wiring circuit boards, or in forming separate interconnect structures that are later added to semiconductor devices or printed circuit wiring boards. Metals that can be both electroplated and planarized in an aqueous metal salt solution are compatible with this process and include copper, silver, nickel, gold, and others, however, copper is the metal of choice for semiconductors.

DEPC:
The Damascene Process

CCXR:
[illegible]

ORPL:
P. Singer, "Making the Move to Dual Damascene Processing," Semiconductor International pp. 79-81, Aug. 1997.

same process on any material that had a conductive seed layer and feature trenches and vias, such as decorative damascene inlays, damascene structures used in printed wiring circuit boards, or in forming separate interconnect structures that are later added to semiconductor devices or printed circuit wiring boards. Metals that can be both electroplated and planarized in an aqueous metal salt solution are compatible with this process and include copper, silver, nickel, gold, and others, however, copper is the metal of choice for semiconductors.

The above description has been that of a preferred embodiment of the present invention. It will occur to those that practice the art that many modifications may be made without departing from the spirit and scope of the invention. For example, the system could be operated in a programmed voltage mode instead of a programmed current mode with the voltage between the anode and cathode controlled by the system computer and programmable controller. In order to apprise the public of the various embodiments that may fall within the scope of the invention the following claims are made.

We claim:

1. A method of bipolar concurrent metal plating and planarizing of a metallized surface of a semiconductor wafer, the method including the steps of:

(a) positioning a bipolar electrode assembly proximate to said metallized surface, said bipolar electrode assembly having an anode and cathode separated along an axis parallel to said metallized surface;

(b) bathing a region between said anode and said cathode and said metallized surface in an electroplating solution;

(c) providing relative motion between said bipolar electrode assembly and said metallized surface, said relative motion being parallel to said metallized surface; and

(d) applying a voltage across said anode and said cathode to plate metal from said electroplating solution onto a first region of said metallized surface; said first region being adjacent to said anode; and to concurrently electropolish said metal from a second region of said metallized surface; said second region being adjacent to said cathode; through the action of flowing current from said anode through said electroplating solution to said first region of said metallized surface, flowing said current through said metallized surface to said second region, and flowing said current to said cathode through said electroplating solution.

2. The method according to claim 1, wherein said relative motion is provided by holding said metallized surface stationary and moving said bipolar electrode assembly.

3. The method according to claim 1, wherein said relative motion is provided by holding said bipolar electrode assembly stationary and moving said metallized surface.

4. The method according to claim 1, wherein said relative motion is provided by moving both said metallized surface and said bipolar electrode assembly.

5. The method according to claim 1, wherein said relative motion is selected from the group consisting of: linear motion, orbital motion, circular motion; and a combination of linear and circular motions.

6. The method according to claim 1, wherein the step of bathing a region between said anode and said cathode and said metallized surface in an electroplating solution is performed via separate supply lines providing different electrolytic solutions proximate the anode and cathode.

7. The method according to claim 1, including the step of positioning a brush between said bipolar electrode assembly and said metallized surface with a surface of said brush adjacent to said metallized surface.

8. The method according to claim 1, wherein said voltage across said anode and said cathode is controlled in accordance with a direction of said relative motion.

9. The method according to claim 1, wherein said flowing current is controlled in accordance with a direction of said relative motion.

10. The method according to claim 1, including the step of supporting said metallized surface from a side opposite said metallized surface.

11. The method according to claim 1, including the step of reusing said electroplating solution by recirculation means and conditioning means.

12. The method according to claim 11, wherein said conditioning means is selected from the group consisting of: heating means, cooling means, chemical modification means, and means for filtration of said electroplating solution.

13. The method according to claim 1, wherein said relative motion is chosen from the group consisting of: linear motion, orbital motion, circular motion; and a combination of linear and circular motions.

14. The method according to claim 1, wherein said relative motion is chosen from the group consisting of: linear motion, orbital motion, circular motion; and a combination of linear and circular motions.

15. The method according to claim 1, wherein said relative motion is selected from the group consisting of: linear motion, orbital motion, circular motion; and a combination of linear and circular motions.

16. A method of bipolar concurrent metal plating and electropolishing of a metallized surface, the method including the steps of:

(a) positioning a bipolar electrode assembly proximate to said metallized surface, said bipolar electrode assembly having an anode and cathode separated along an axis parallel to said metallized surface;

(b) bathing a region between said anode and said cathode and said metallized surface in an electroplating solution;

(c) providing relative motion between said bipolar electrode assembly and said metallized surface, said relative motion being parallel to said metallized surface; and

(d) applying a voltage across said anode and said cathode to plate metal from said electroplating solution onto a first region of said metallized surface; said first region being adjacent to said anode; and to concurrently electropolish said metal from a second region of said metallized surface; said second region being adjacent to said cathode; through the action of flowing current from said anode through said electroplating solution to said first region of said metallized surface, flowing said current through said metallized surface to said second region, and flowing said current to said cathode through said electroplating solution.

17. The method according to claim 16, wherein said relative motion is provided by holding said metallized surface stationary and moving said bipolar electrode assembly.

18. The method according to claim 16, wherein said relative motion is provided by holding said bipolar electrode assembly stationary and moving said metallized surface.

19. The method according to claim 16, wherein said relative motion is provided by moving both said metallized surface and said bipolar electrode assembly.

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10	US 6126806 A	17							☑				USPAT
11	US 6107186 A	10							☑				USPAT
12	US 6099712 A	59						☑					USPAT

DOCUMENT-IDENTIFIER: US 6107186 A
TITLE: High planarity high-density in-laid metallization patterns by damascene -CMP processing

---------- RWIC ---------

TTL:
High planarity high-density in-laid metallization patterns by damascene -CMP processing

ABPL:
Erosion of high density metallization areas associated with conventional damascene -CMP processing is avoided and greater planarity achieved by selectively increasing the metal overburden layer thickness at high density metallization regions. Embodiments include initially filling recesses formed in the substrate surface with a metal forming a blanket or overburden layer of the metal thereon. Regions of the blanket or overburden layer overlying regions of high density metallization are selectively electroplated to a greater thickness. The surface is then planarized by CMP, with the selectively increased thickness areas of the overburden layer compensating for greater erosion rates thereat during CMP, thereby resulting in greater planarity of the polished surface.

BSPR:
This invention relates to a method for forming metal films as part of high-density metallization processing of particular utility in integrated circuit semiconductor device and circuit board manufacture, which process employs "damascene " (or "in-laid") technology.

BSPR:
Metal films of the type contemplated herein are used, e.g., in "back-end" semiconductor manufacturing technology, to form electrically conductive contacts to active as well as passive device regions or components formed in or on a semiconductor substrate, as well as for filling via holes, interlevel metallization, and interconnection routing patterns for wiring together the components and/or regions. Metals employed for such purposes include, inter alia, titanium, tantalum, tungsten, aluminum, chromium, nickel, cobalt, silver, gold, copper, and their alloys. Of these, copper and copper-based alloys are particularly attractive for use in large-scale integration (LSI), very large-scale integration (VLSI), and ultra large-scale integration (ULSI) semiconductor devices requiring multilevel metallization systems for "back-end" processing of the semiconductor wafers on which the devices are based. Copper and copper-based metallization systems have very low resistivities, i.e., lower than those of previously preferred systems utilizing aluminum and its alloys, as well as significantly higher resistance to electromigration. Moreover, copper and its alloys enjoy a considerable cost advantage over a number of the above-enumerated metals, notably silver and gold . Also, in contrast to aluminum and the refractory-type metals included in the above listing, copper and its alloys can be readily deposited in good quality, bright layer form by well-known electroplating techniques, at deposition rates fully compatible with the requirements of device manufacturing throughput.

BSPR:
Referring now to FIG. 1, schematically shown therein in cross-sectional view is a conventional damascene processing sequence for forming recessed (i.e.,

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United States Patent [19]

Erb

[11] Patent Number: 6,107,186

[45] Date of Patent: Aug. 22, 2000

[54] HIGH PLANARITY HIGH-DENSITY IN-LAID METALLIZATION PATTERNS BY DAMASCENE-CMP PROCESSING

[75] Inventor: Darrell M. Erb, Los Altos, Calif.

[73] Assignee: Advanced Micro Devices, Inc., Sunnyvale, Calif.

[21] Appl. No.: 09/238,051

[22] Filed: Jan. 27, 1999

[51] Int. Cl.[7] H01L 21/4763

[52] U.S. Cl. 438/633; 438/587; 438/692; 427/98; 427/99; 427/250; 427/430.1; 427/443.1; 205/95; 205/103; 205/104; 205/118; 205/123; 205/125

[58] Field of Search 205/95, 123, 103, 205/104, 118, 125; 438/692, 633, 687; 216/88; 427/98, 99, 250, 430.1, 443.1

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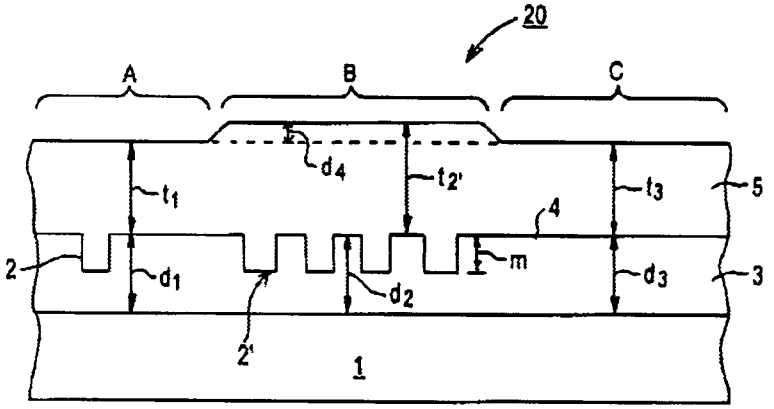
Primary Examiner—Kathryn Gorgos
Assistant Examiner—Christopher M. Keehan

[57] ABSTRACT

Erosion of high density metallization areas associated with conventional damascene-CMP processing is avoided and greater planarity achieved by selectively increasing the metal overburden layer thickness at high density metallization regions. Embodiments include initially filling recesses formed in the substrate surface with a metal forming a blanket or overburden layer of the metal thereon. Regions of the blanket or overburden layer overlying regions of high density metallization are selectively electroplated to a greater thickness. The surface is then planarized by CMP, with the selectively increased thickness areas of the overburden layer compensating for greater erosion rates thereat during CMP, thereby resulting in greater planarity of the polished surface.

19 Claims, 3 Drawing Sheets



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8	US 6143155 A	17											USPAT
9	US 6132586 A	18											USPAT
10	US 6126806 A	17											USPAT
11	US 6107186 A	10											USPAT
12	US 6099712 A	59											USPAT
13	US 6056864 A	6											USPAT
14	US 6004880 A	9											USPAT

DOCUMENT-IDENTIFIER: US 6056864 A
TITLE: Electropolishing copper film to enhance CMP throughput

---------- KWIC ---------

ABPL:
In-laid metal, e.g., copper or copper alloy, contacts and conductive routing patterns are formed in recesses in the surface of a substrate by a damascene -type process, comprising depositing a layer of an electrically conductive material filling the recesses and covering the substrate surface, reducing the thickness of the layer by a process providing a faster rate of layer removal than that obtained by chemical-mechanical polishing (CMP), and subjecting the remaining layer thickness to CMP processing to (a) substantially remove the remaining layer thickness and (b) render the exposed upper surface of the material filling the recesses substantially coplanar with the substrate surface, whereby increased manufacturing throughput, greater planarity, and reduced defects are obtained.

BSPR:
This invention relates to metallization processes of particular utility in integrated semiconductor device and circuit board manufacture, which processes employ "damascene " (or in-laid) technology.

BSPR:
With reference to FIG. 1, schematically shown therein in cross-sectional view is a conventional damascene processing sequence for forming recessed metallization patterns ("back-end" contacts, vias, interconnections, etc.) in semiconductor devices formed in or on a semiconductor wafer substrate 1. In a first step, the desired conductor pattern is defined as a pattern of recesses 2 such as grooves, trenches, holes, etc. in a dielectric layer 3 formed over the semiconductor substrate, followed by a second step comprising deposition of a suitably conductive metal layer 5 filling the etched recesses 2. Typically, in order to ensure complete filling of the recesses, the metal layer 5 is deposited as a blanket layer of excess thickness t so as to overfill the recesses 2 and cover the upper surface 4 of the dielectric layer 3. Next, the entire excess thickness t of metal layer 5 over the surface of the dielectric layer 3 is removed using a CMP process, leaving metal portions 5' in the recesses with their upper (i.e., exposed) surfaces 6 substantially coplanar with the surface 4 of the dielectric layer. Thus this process, termed "damascene process", forms in-laid conductors in the dielectric layer while avoiding problems associated with types of other processes, e.g., metal etching and dielectric gap filling.

BSPR:
While such damascene processing can be performed with a variety of other types of substrates, e.g., printed circuit boards, with and/or without intervening dielectric layers, and with a number of metallization materials, including copper, aluminum, gold, silver, and their alloys, the parallel drives toward cost reduction and increased microminiaturization of semiconductor devices have provided an impetus for greater utilization of copper or copper alloy-based interconnection metallurgy, particularly in view of the attendant low resistivity and ability to reliably carry high current densities. However, the use of copper-based metallurgy has presented several problems, including the possibility of diffusion into the semiconductor substrate and poor adhesion to various dielectric materials, necessitating provision of an adhesion/barrier

United States Patent [19]

Cheung

[11] Patent Number: 6,056,864

[45] Date of Patent: May 2, 2000

[54] ELECTROPOLISHING COPPER FILM TO ENHANCE CMP THROUGHPUT

[75] Inventor: Robin W. Cheung, Cupertino, Calif.

[73] Assignee: Advanced Micro Devices, Inc., Sunnyvale, Calif.

[21] Appl. No.: 09/170,220

[22] Filed: Oct. 13, 1998

[51] Int. Cl.[7] C25D 5/52; C25D 5/48; C23C 16/00; H01L 21/20; H01L 21/302

[52] U.S. Cl. 205/222; 205/157; 205/223; 427/250; 427/355; 427/331; 438/564; 438/692; 438/697; 438/758; 438/618

[58] Field of Search 205/157, 222, 205/223; 427/250, 355, 331; 438/618, 692, 694, 758, 759, 697

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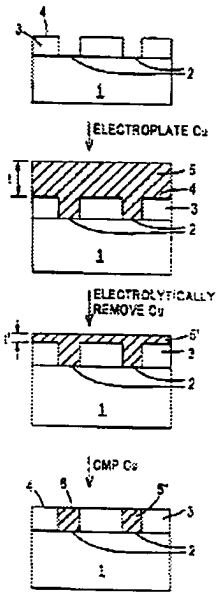
Primary Examiner—Kathryn Gorgos
Assistant Examiner—Edna Wong

[57] ABSTRACT

In-laid metal, e.g., copper or copper alloy, contacts and conductive routing patterns are formed in recesses in the surface of a substrate by a damascene-type process, comprising depositing a layer of an electrically conductive material filling the recesses and covering the substrate surface, reducing the thickness of the layer by a process providing a faster rate of layer removal than that obtained by chemical-mechanical polishing (CMP), and subjecting the remaining layer thickness to CMP processing to (a) substantially remove the remaining layer thickness and (b) render the exposed upper surface of the material filling the recesses substantially coplanar with the substrate surface, whereby increased manufacturing throughput, greater planarity, and reduced defects are obtained.

17 Claims, 1 Drawing Sheet



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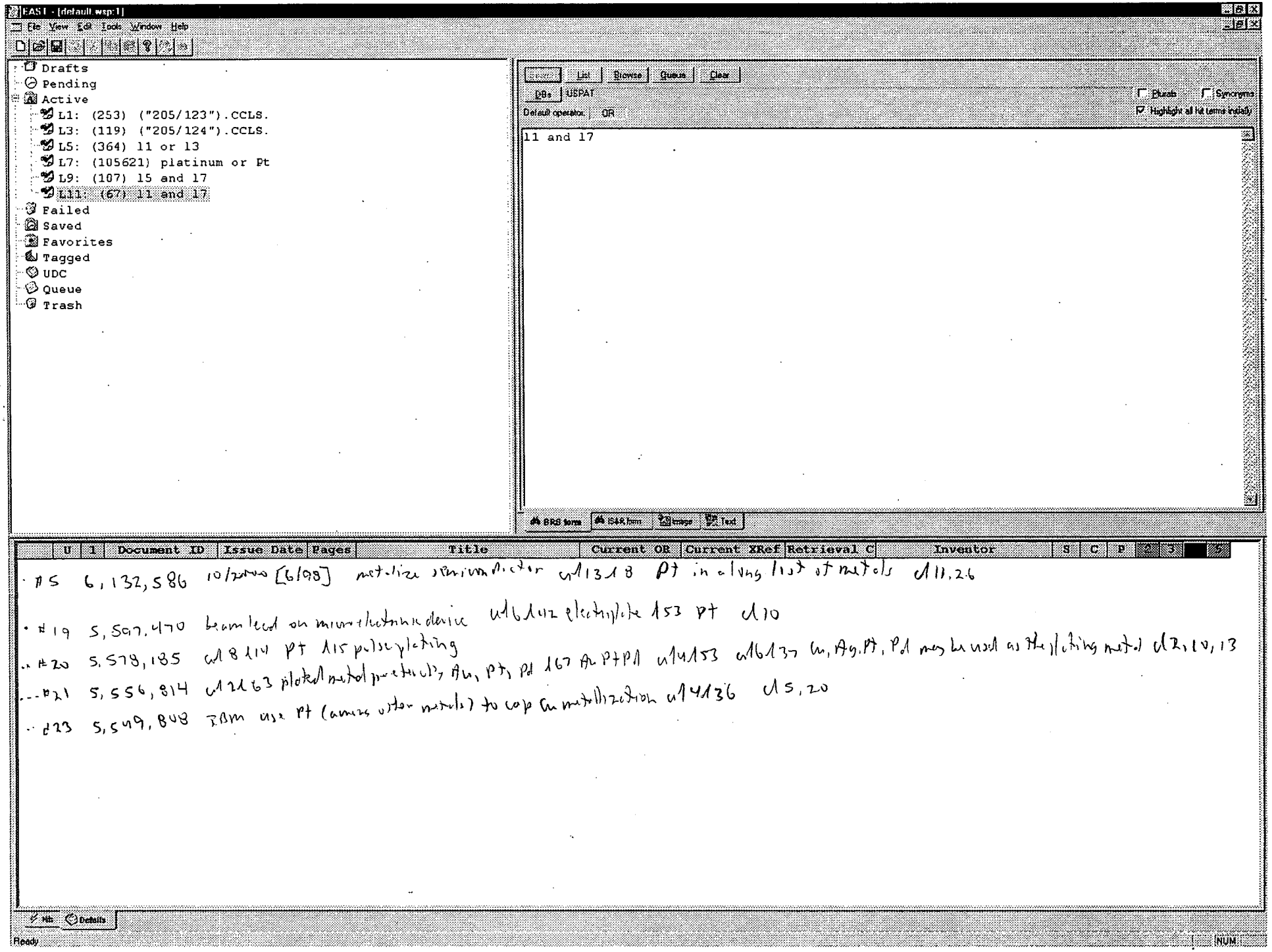


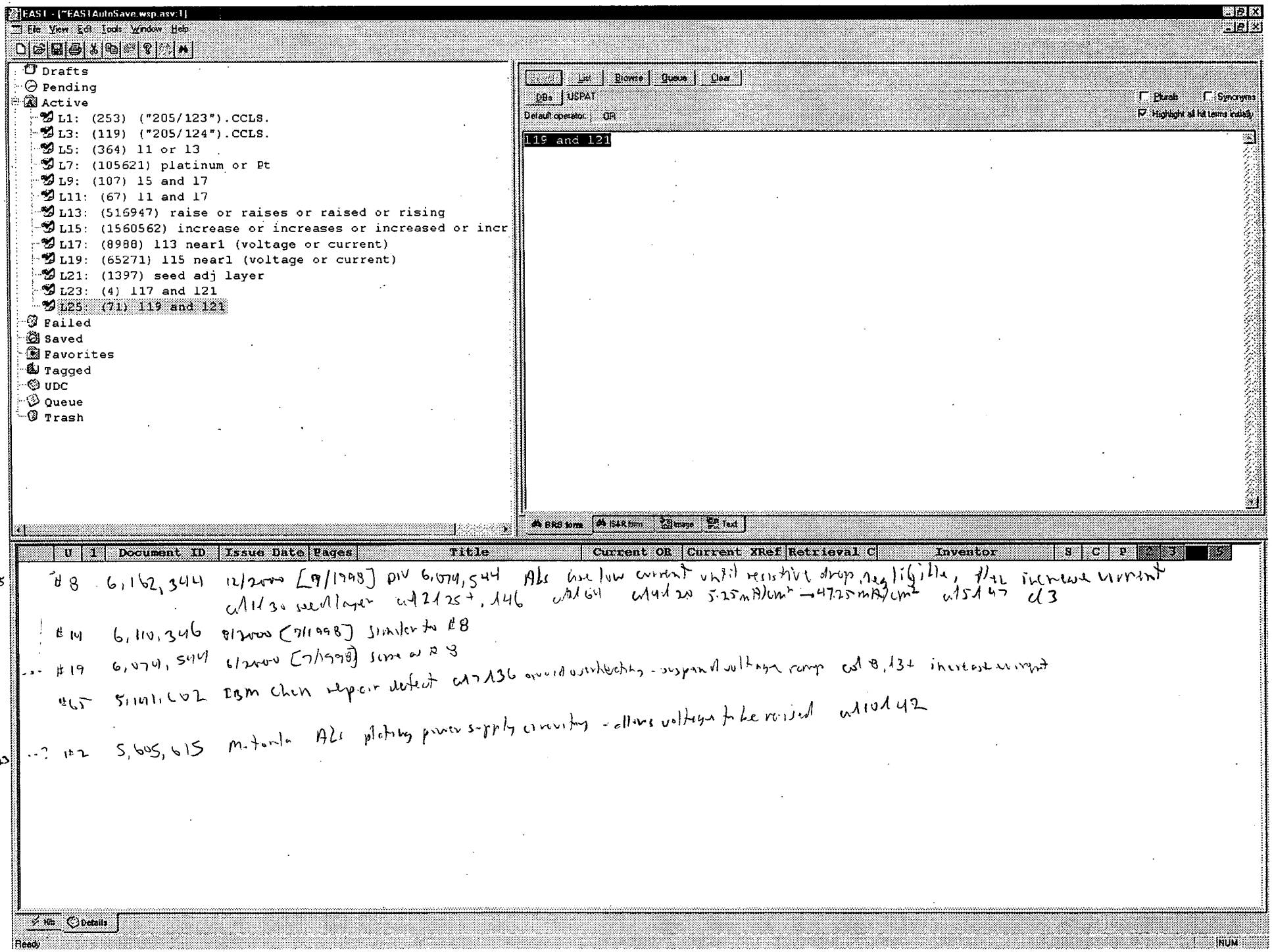
#5 6,132,586 10/2000 [6/98] metalize semiconductor u/1318 Pt in a long list of metals cl1,2,6

#19 5,507,470 beam lead on microelectronic device u/6402 electroplate 153 Pt cl10

#20 5,578,185 u/8114 Pt 115 pulse plating

#21 5,556,814 u/2163 plated metal protection Au, Pt, Pd 167 Au Pt Pd u/4153 u/6137 Cu, Ag, Pt, Pd may be used as the plating metal cl2,10,13

#23 5,549,808 IBM use Pt (among other metals) to cap Cu metallization u/4136 cl5,20



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#8 6,162,344 12/2000 [9/1998] DIV 6,074,544 Abs use low current until resistive drop negligible, then increase current col 1 l 30 seed layer col 2 l 25 +, 146 col 6 l 64 col 9 l 20 5.25 mA/cm² → 47.25 mA/cm² col 15 l 47 cl 3

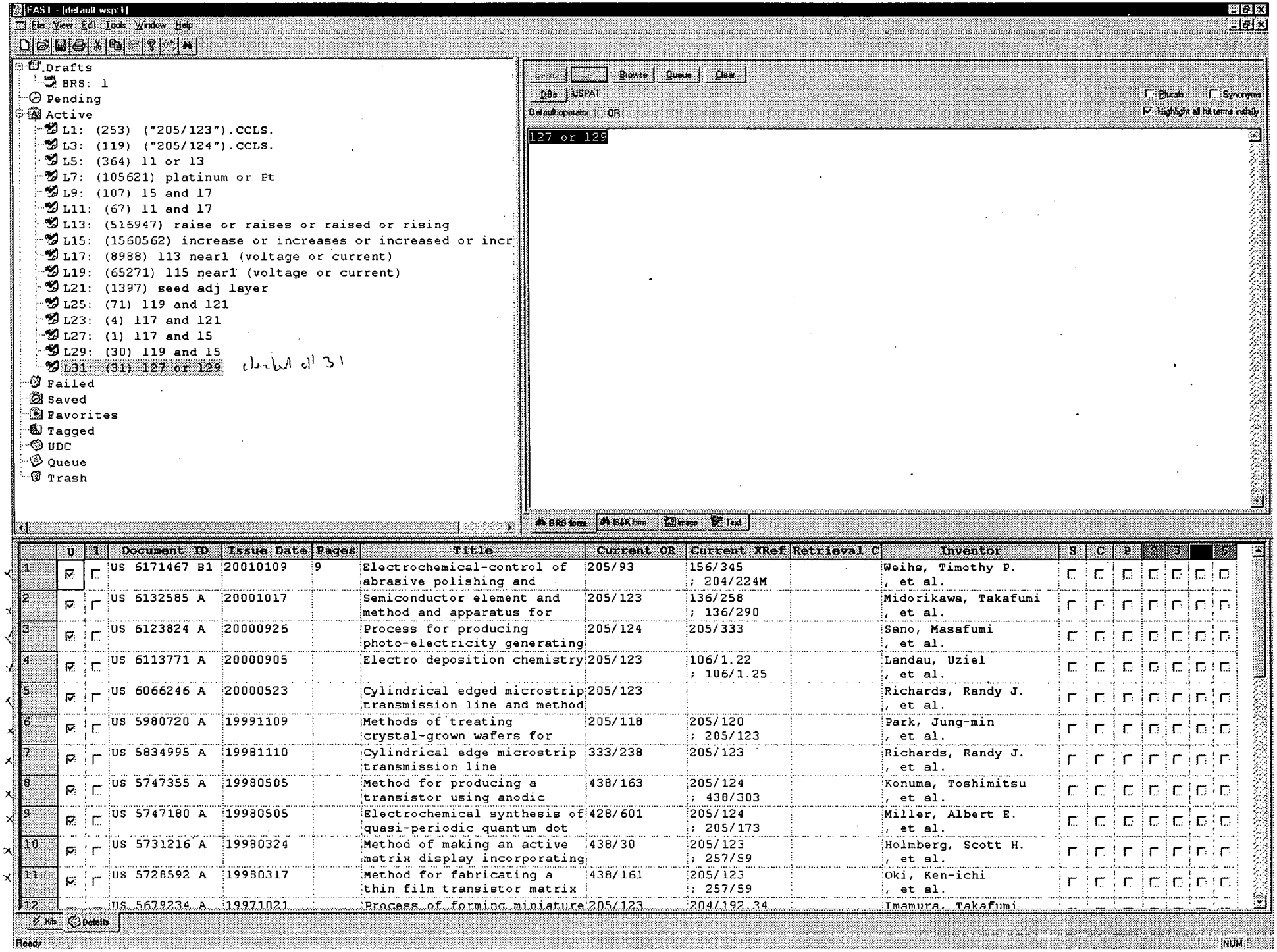
#14 6,110,346 8/2000 [7/1998] similar to #8

#19 6,074,544 6/2000 [7/1998] same as # 8

#65 5,141,602 IBM Chen repair defect col 7 l 36 avoid overshooting - suspend voltage ramp col 8, l 3+ increase current

line 33

#2 5,605,615 Motorola Abs plating power supply circuitry - allows voltage to be raised col 10 l 42



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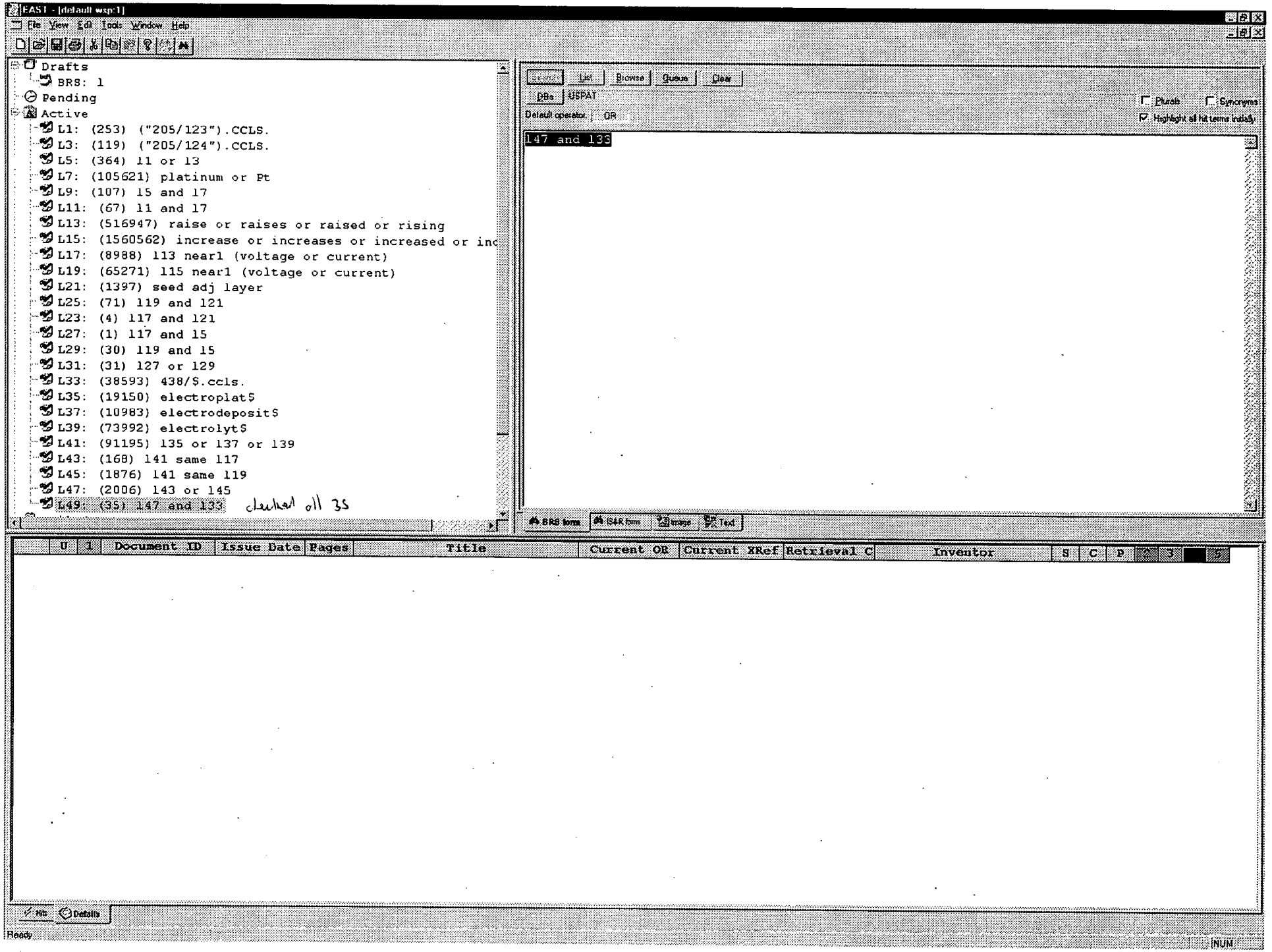
1	☑	☐	US 6171467 B1	20010109	9	Electrochemical-control of abrasive polishing and	205/93	156/345 ; 204/224M		Weihs, Timothy P. , et al.	☐	☐	☐	☐	☐	☐	☐
2	☑	☐	US 6132585 A	20001017		Semiconductor element and method and apparatus for	205/123	136/258 ; 136/290		Midorikawa, Takafumi , et al.	☐	☐	☐	☐	☐	☐	☐
3	☑	☐	US 6123824 A	20000926		Process for producing photo-electricity generating	205/124	205/333		Sano, Masafumi , et al.	☐	☐	☐	☐	☐	☐	☐
4	☑	☐	US 6113771 A	20000905		Electro deposition chemistry	205/123	106/1.22 ; 106/1.25		Landau, Uziel , et al.	☐	☐	☐	☐	☐	☐	☐
5	☑	☐	US 6066246 A	20000523		Cylindrical edged microstrip transmission line and method	205/123			Richards, Randy J. , et al.	☐	☐	☐	☐	☐	☐	☐
6	☑	☐	US 5980720 A	19991109		Methods of treating crystal-grown wafers for	205/118	205/120 ; 205/123		Park, Jung-min , et al.	☐	☐	☐	☐	☐	☐	☐
7	☑	☐	US 5834995 A	19981110		Cylindrical edge microstrip transmission line	333/238	205/123		Richards, Randy J. , et al.	☐	☐	☐	☐	☐	☐	☐
8	☑	☐	US 5747355 A	19980505		Method for producing a transistor using anodic	438/163	205/124 ; 438/303		Konuma, Toshimitsu , et al.	☐	☐	☐	☐	☐	☐	☐
9	☑	☐	US 5747180 A	19980505		Electrochemical synthesis of quasi-periodic quantum dot	428/601	205/124 ; 205/173		Miller, Albert E. , et al.	☐	☐	☐	☐	☐	☐	☐
10	☑	☐	US 5731216 A	19980324		Method of making an active matrix display incorporating	438/30	205/123 ; 257/59		Holmberg, Scott H. , et al.	☐	☐	☐	☐	☐	☐	☐
11	☑	☐	US 5728592 A	19980317		Method for fabricating a thin film transistor matrix	438/161	205/123 ; 257/59		Oki, Ken-ichi , et al.	☐	☐	☐	☐	☐	☐	☐
12			US 5679234 A	19971021		Process of forming miniature	205/123	204/192.34		Imamura, Takafumi							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L7: (105621) platinum or Pt
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L15: (1560562) increase or increases or increased or inc
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L19: (65271) l15 near1 (voltage or current)
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Pages
Title
Current OR
Current XRef
Retrieval C
Inventor
S
C
P
Hits
Details
Ready
NUM

- Drafts
- Pending
- Active
  - L1: (77647) wafer or wafers
  - L2: (83347) spin or spun
  - L3: (1735) l2 near2 dry
  - L4: (427) l1 and l3
  - L5: (281) l1 same l3
  - L6: (86905) rinse or rinses or rinsed or rinsing
  - L7: (213) l6 same l5
  - L8: (13209) 205/50-333.ccls.
  - L9: (6) l7 and l8
- Failed
- Saved
- Favorites
- Tagged
- UDC
- Queue
- Trash

Browse | Queue | Clear

DBs: USPAT

Default operator: OR

Plurals | Synonyms | Highlight all hit terms initially

l7 and l8

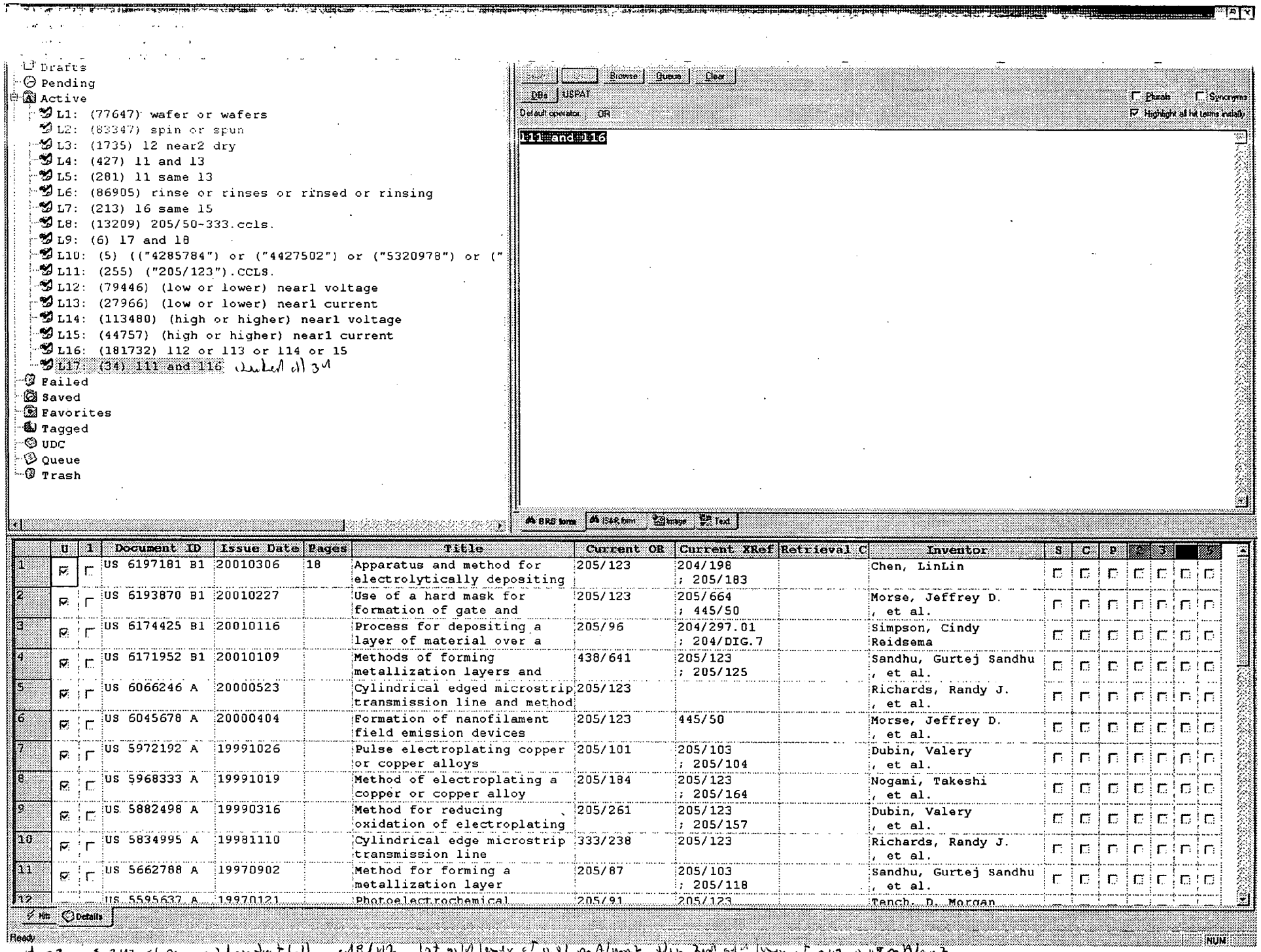
BRS form | IS&R form | Image | Text

	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval C	Inventor	S	C	P	?	?		
1	☑	☐	US 6179982 B1	20010130	26	Introducing and reclaiming liquid in a wafer processing	205/80	204/224M ; 204/224R		Ting, Chiu H. , et al.	☐	☐	☐	☐	☐	☐	☐
2	☑	☐	US 6077412 A	20000620		Rotating anode for a wafer processing chamber	205/143	204/212 ; 204/224M		Ting, Chiu H. , et al.	☐	☐	☐	☐	☐	☐	☐
3	☑	☐	US 5755944 A	19980526		Formation of layer having openings produced by	204/486	204/490 ; 204/492		Haven, Duane A. , et al.	☐	☐	☐	☐	☐	☐	☐
4	☑	☐	US 5545307 A	19960813		Process for patterned electroplating	205/122	430/320		Doss, Saad K. , et al.	☐	☐	☐	☐	☐	☐	☐
5	☑	☐	US 5516418 A	19960514		Patterned electroplating	205/119	205/122 ; 205/135		Doss, Saad K. , et al.	☐	☐	☐	☐	☐	☐	☐
6	☑	☐	US 4514254 A	19850430		Groundplane post-etch anodization	205/125	205/189 ; 205/322		Klepner, Stephen P.	☐	☐	☐	☐	☐	☐	☐

Hits | Details

Ready

NUM



	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval C	Inventor	S	C	P	2	3		6
1	☑	☐	US 6197181 B1	20010306	18	Apparatus and method for electrolytically depositing	205/123	204/198 ; 205/183		Chen, LinLin	☐	☐	☐	☐	☐	☐	☐
2	☑	☐	US 6193870 B1	20010227		Use of a hard mask for formation of gate and	205/123	205/664 ; 445/50		Morse, Jeffrey D. , et al.	☐	☐	☐	☐	☐	☐	☐
3	☑	☐	US 6174425 B1	20010116		Process for depositing a layer of material over a	205/96	204/297.01 ; 204/DIG.7		Simpson, Cindy Reidsema	☐	☐	☐	☐	☐	☐	☐
4	☑	☐	US 6171952 B1	20010109		Methods of forming metallization layers and	438/641	205/123 ; 205/125		Sandhu, Gurtej Sandhu , et al.	☐	☐	☐	☐	☐	☐	☐
5	☑	☐	US 6066246 A	20000523		Cylindrical edged microstrip transmission line and method	205/123			Richards, Randy J. , et al.	☐	☐	☐	☐	☐	☐	☐
6	☑	☐	US 6045678 A	20000404		Formation of nanofilament field emission devices	205/123	445/50		Morse, Jeffrey D. , et al.	☐	☐	☐	☐	☐	☐	☐
7	☑	☐	US 5972192 A	19991026		Pulse electroplating copper or copper alloys	205/101	205/103 ; 205/104		Dubin, Valery , et al.	☐	☐	☐	☐	☐	☐	☐
8	☑	☐	US 5968333 A	19991019		Method of electroplating a copper or copper alloy	205/184	205/123 ; 205/164		Nogami, Takeshi , et al.	☐	☐	☐	☐	☐	☐	☐
9	☑	☐	US 5882498 A	19990316		Method for reducing oxidation of electroplating	205/261	205/123 ; 205/157		Dubin, Valery , et al.	☐	☐	☐	☐	☐	☐	☐
10	☑	☐	US 5834995 A	19981110		Cylindrical edge microstrip transmission line	333/238	205/123		Richards, Randy J. , et al.	☐	☐	☐	☐	☐	☐	☐
11	☑	☐	US 5662788 A	19970902		Method for forming a metallization layer	205/87	205/103 ; 205/118		Sandhu, Gurtej Sandhu , et al.	☐	☐	☐	☐	☐	☐	☐
12			US 5595637 A	19970121		Photoelectrochemical	205/91	205/123		Tench, D. Morgan							

Hits
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Ready
NUM

23 5,242,564 gold contact cell with 1st gold layer of 0.01 mA/mm² plus 2nd gold layer of 0.03-0.05 mA/mm²

File View Edit Tools Window Help

- Drafts
- Pending
- Active
  - L1: (77847) water or wafers
  - L2: (65547) spin or spun
  - L3: (1735) 12 near2 dry
  - L4: (427) 11 and 13
  - L5: (281) 11 same 13
  - L6: (86905) rinse or rinses or rinsed or rinsing
  - L7: (213) 16 same 15
  - L8: (13209) 205/50-333.ccls.
  - L9: (6) 17 and 18
  - L10: (5) (("4285784") or ("4427502") or ("5320978") or
  - L11: (255) ("205/123").CCLS.
  - L12: (79446) (low or lower) near1 voltage
  - L13: (27966) (low or lower) near1 current
  - L14: (113480) (high or higher) near1 voltage
  - L15: (44757) (high or higher) near1 current
  - L16: (181732) 112 or 113 or 114 or 15
  - L17: (34) 111 and 116
  - L18: (13209) 205/50-333.ccls.
  - L19: (15996) 116 same (semiconductor or semiconductors
  - L20: (70) 118 and 119
  - L21: (61) 120 not 117
- Failed
- Saved
- Favorites
- Tagged
- UDC

List | Browse | Queue | Clear

DBs USPAT

Plurals | Synonyms | Highlight all hit terms initially

120 not 117

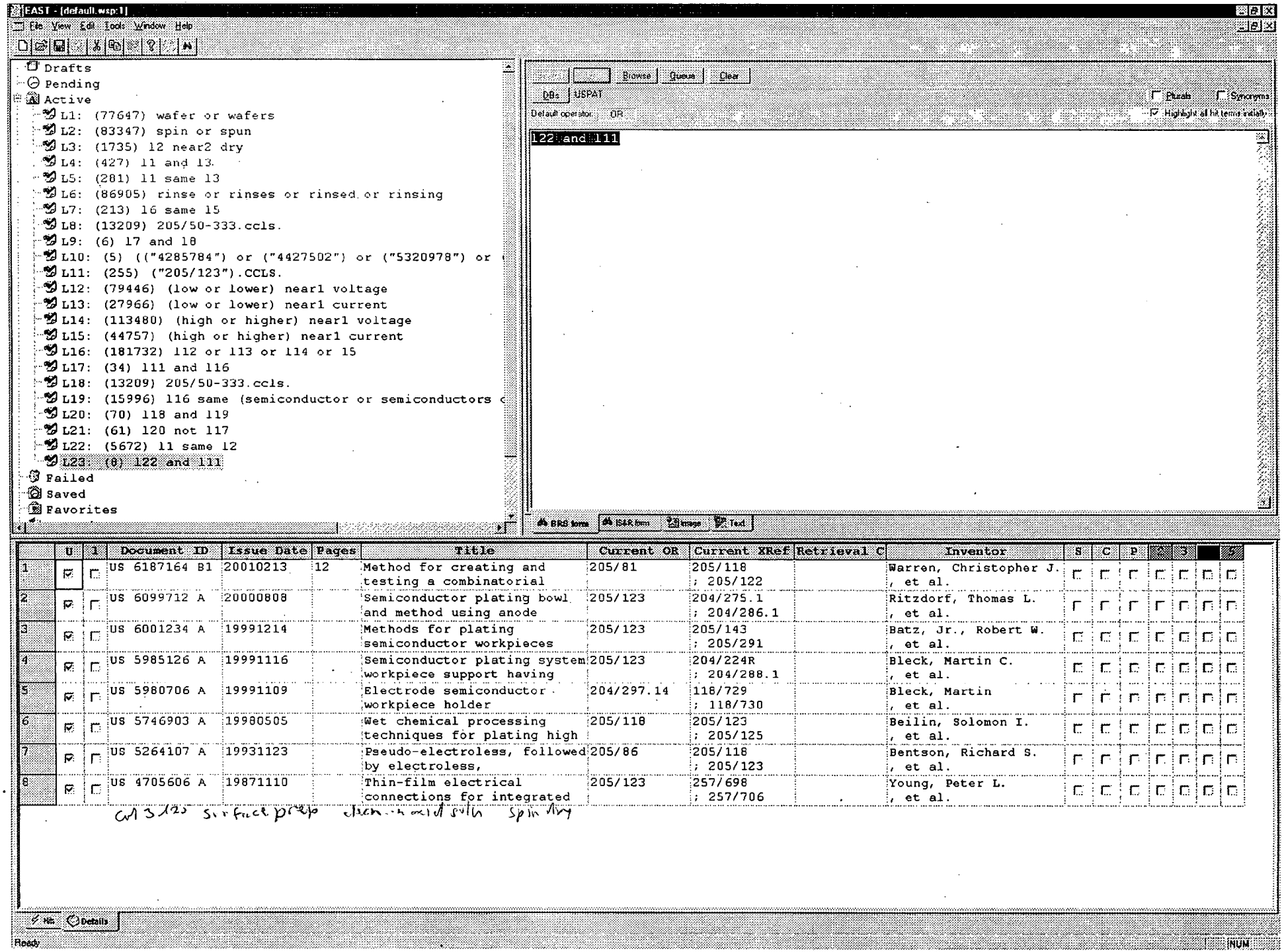
BRS form | IS&R form | Image | Text

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval C	Inventor	S	C	P	2	3		5

..#4 6,140,241 Also deposit Cu in 2 stages low current; then high current w/5 1M+

Hits | Details

Ready NUM



	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval C	Inventor	S	C	P	?	?		?
1	☑	☐	US 6187164 B1	20010213	12	Method for creating and testing a combinatorial	205/81	205/118 ; 205/122		Warren, Christopher J. , et al.	☐	☐	☐	☐	☐	☐	☐
2	☑	☐	US 6099712 A	20000808		Semiconductor plating bowl and method using anode	205/123	204/275.1 ; 204/286.1		Ritzdorf, Thomas L. , et al.	☐	☐	☐	☐	☐	☐	☐
3	☑	☐	US 6001234 A	19991214		Methods for plating semiconductor workpieces	205/123	205/143 ; 205/291		Batz, Jr., Robert W. , et al.	☐	☐	☐	☐	☐	☐	☐
4	☑	☐	US 5985126 A	19991116		Semiconductor plating system workpiece support having	205/123	204/224R ; 204/288.1		Bleck, Martin C. , et al.	☐	☐	☐	☐	☐	☐	☐
5	☑	☐	US 5980706 A	19991109		Electrode semiconductor workpiece holder	204/297.14	118/729 ; 118/730		Bleck, Martin , et al.	☐	☐	☐	☐	☐	☐	☐
6	☑	☐	US 5746903 A	19980505		Wet chemical processing techniques for plating high	205/118	205/123 ; 205/125		Beilin, Solomon I. , et al.	☐	☐	☐	☐	☐	☐	☐
7	☑	☐	US 5264107 A	19931123		Pseudo-electroless, followed by electroless,	205/86	205/118 ; 205/123		Bentson, Richard S. , et al.	☐	☐	☐	☐	☐	☐	☐
8	☑	☐	US 4705606 A	19871110		Thin-film electrical connections for integrated	205/123	257/698 ; 257/706		Young, Peter L. , et al.	☐	☐	☐	☐	☐	☐	☐

cl 3 125 surface prep clean + acid soln spin dry